LINEAR INTEGRATED CIRCUIT

TDA1770

PRELIMINARY DATA

VERTICAL DEFLECTION CIRCUIT

The TDA 1770 is a monolithic integrated circuit in 20-lead plastic package. It is a full performance and very efficient vertical deflection circuit intended for direct drive of the yoke.
It offers a wide range of applications in portable CTVs, BW TVs, monitors and displays. The functions incorporated are:

- synchronization circuit.
- precision oscillator and ramp generator
- power output amplifier
- flyback generator
- voltage regulator
- precision blanking pulse generator
- thermal shut down protection
- CRT screen protection circuit which blanks the beam current in the event of loss of vertical deflection current.

The TDA 1770 is assembled in a new 20-lead plastic package which has 4 centre pins connected together and used for heatsinking.

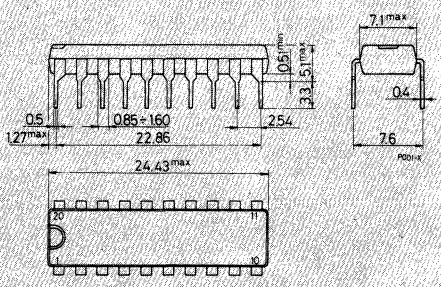
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage at pin 2	35	V
V_7, V_8	Flyback peak voltage	60	V
V_{11}	Sync. input voltage	20	V
V_{19}, V_{20}	Power amplifier input voltage	V_s / -10	V
V_1	Voltage at pin 1	V_s	
I_o	Output current (non repetitive) at t = 2 msec	2	A
I_o	Output peak current at f = 50 Hz t > 10 μsec	1.2	A
I_o	Output peak current at f = 50 Hz t ⩽ 10 μsec	2.2	A
I_3	Pin 3 peak to peak flyback current at f = 50 Hz, t_{fly} ⩽ 1.5 msec	2	A
I_3	Pin 3 DC current at $V_7 < V_2$	50	mA
P_{tot}	Maximum power dissipation: at T_{pins} ⩽ 90°C	4.3	W
	at T_{amb} = 70°C	1	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

ORDERING NUMBER: TDA 1770

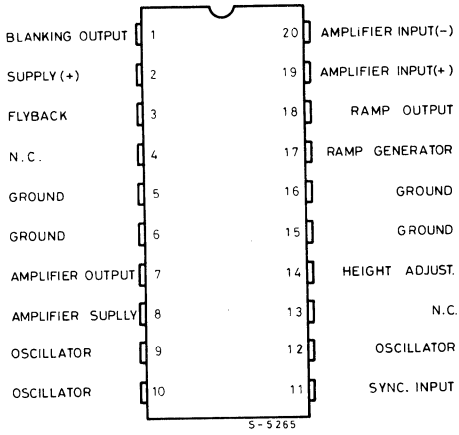
MECHANICAL DATA

Dimensions in mm

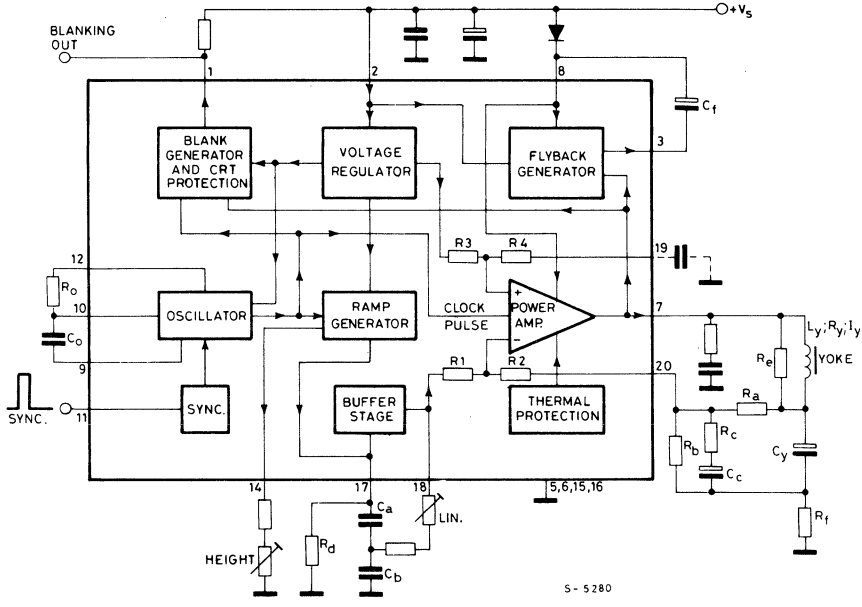


TDA1770

CONNECTION DIAGRAM
(top view)



BLOCK DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}pins}$	Thermal resistance junction-pins	max	14	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	80	°C/W

ELECTRICAL CHARACTERISTICS (V_s= 35V, T_{amb}= 25°C, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit	Fig.
DC CHARACTERISTICS							
I_2	Pin 2 quiescent current			30	50	mA	1b
I_8	Pin 8 quiescent current	I_7= 0		18	30	mA	1b
$-I_{17}$	Ramp generator bias current	V_{17}= 0		0.02	1	μA	1a
$-I_{17}$	Ramp generator current	V_{17}= 0; $-I_{14}$= 20 μA	18.5	20	21.5	μA	1b
$\left\lvert\frac{\Delta I_{17}}{I_{17}}\right\rvert$	Ramp generator non linearity	ΔV_{17}= 0 to 15V $-I_{14}$= 20 μA		0.2	1	%	1b
V_1	Blanking output saturation voltage	I_1= 10 mA		0.35		V	1b
V_3	Pin 3 saturation voltage to ground	I_3= 20 mA		1	1.3	V	1a
V_7	Quiescent output voltage	V_s= 35V; R_a= 2.2 KΩ R_b= 1 KΩ	16.8	17.8	18.6	V	1a
		V_s= 15V; R_a= 390Ω R_b= 1 KΩ	7.1	7.5	8	V	
V_{7L}	Output saturation voltage to ground	I_7= 0.7A		0.7	1	V	1c
V_{7H}	Output saturation voltage to supply	$-I_7$= 0.7A		1.3	1.8	V	1d
V_{10}	Oscillator virtual ground			0.45		V	1a
V_{14}	Regulated voltage at pin 14	$-I_{14}$= 20 μA	6.3	6.6	7.1	V	1b
$\frac{\Delta V_{14}}{\Delta V_s}$	Regulated voltage drift with supply voltage	ΔV_s= 15 to 35V		1		$\frac{mV}{V}$	1b
V_{19}	Amplifier input (+) reference voltage		4.2	4.4	4.6	V	1b

Fig. 1 - DC test circuit

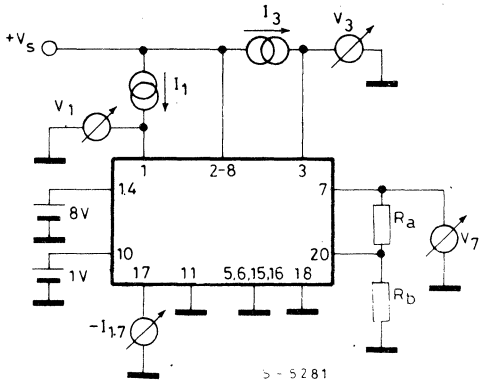


Fig. 1a

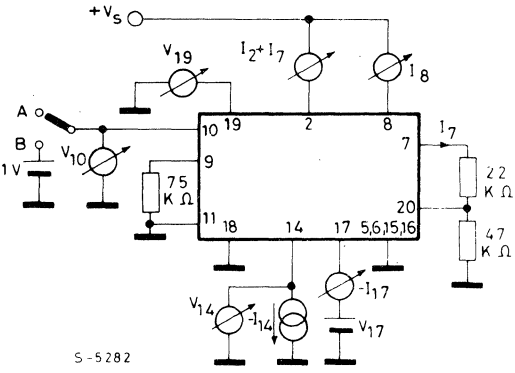


Fig. 1b

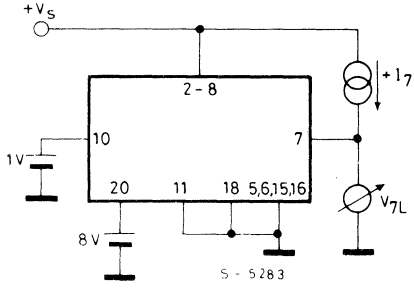


Fig. 1c

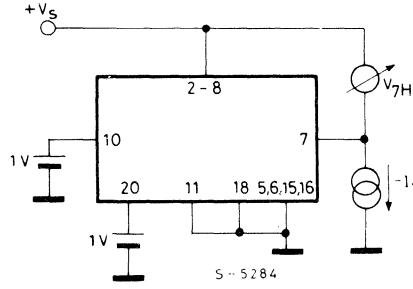


Fig. 1d

ELECTRICAL CHARACTERISTICS (Refer to the A.C. test circuit of fig. 2, V_s= 20V, f= 50 Hz, T_{amb}= 25°C, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
AC CHARACTERISTICS						
I_s	Supply current	I_y= 1 App		160		mA
I_{11}	Sync. input current		100			μA
V_7	Flyback voltage	I_y= 1 App		42		V
V_9	Peak to peak oscillator sawtooth voltage	I_{11}= 0		3.6		V
		I_{11}= 100 μA		3.4		V
V_{18thL}	Start scan level of the input ramp			1.85		V
t_{fly}	Flyback time	I_y= 1 App		0.75		msec
t_{blank}	Blanking pulse duration	f_o= 50 Hz		1.4		ms
		f_o= 60 Hz		1.17		ms
f_o	Free running frequency	R_o= 7.5 KΩ C_o= 330 nF		43.5		Hz
		R_o= 6.2 KΩ C_o= 330 nF		52.5		Hz
Δf	Synchronization range	I_{11}= 100 μA		16		Hz
T_j	Junction temperature for thermal shut-down			145		°C

Fig. 2 - AC test circuit

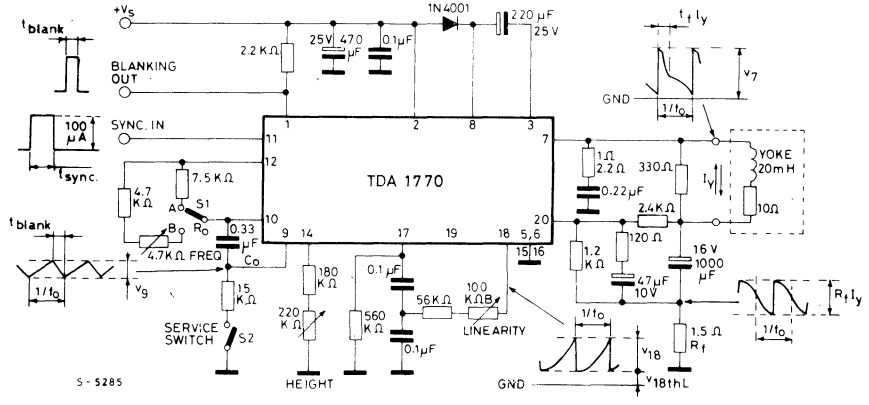
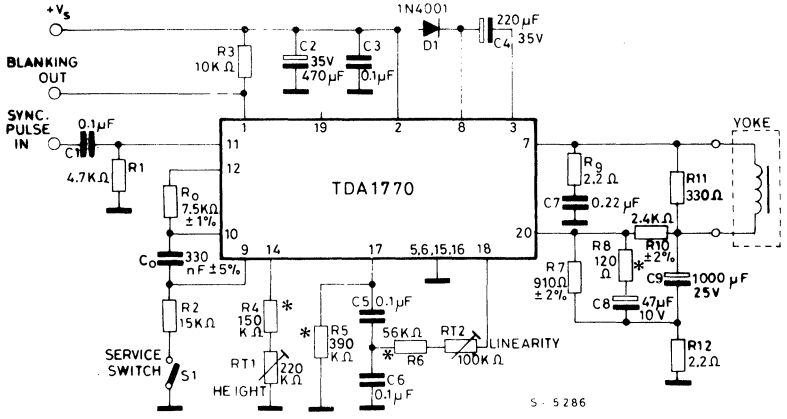


Fig. 3 - Typical application circuit for small screen 90° TVC set (Ry= 15Ω; Ly= 30 mH; Iy= 0.82 App)



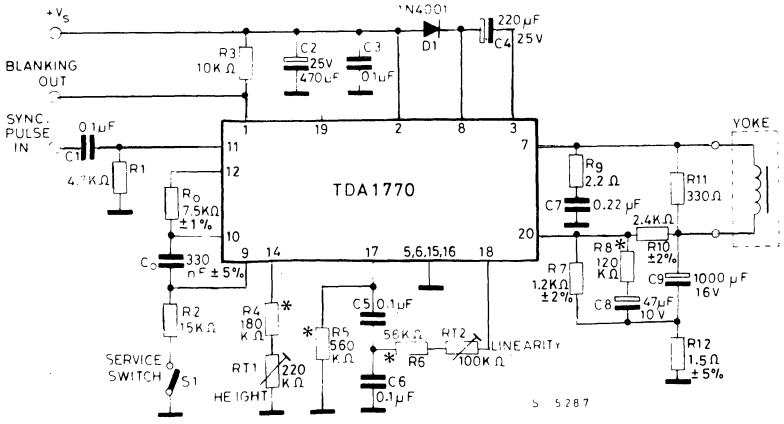
* The value depends on the characteristics of the CRT. The value shown is indicative only.

Typical performance

V_s	Minimum supply voltage	25	V
I_s	Supply current	140	mA
t_{fly}	Flyback time	0.7	msec
t_{blkg}	Blanking time	1.4	msec
f_o	Free running frequency	43.5	Hz
P_{tot}	Total dissipation	2.4	W
$R_{th\ heatsink}$ **	Thermal resistance of the heatsink for T_{amb}= 60°C and $T_{j\ max}$= 130°C	8	°C/W

** See "Thermal considerations".

Fig. 4 - Typical application circuit for B/W TV set (Ry= 10Ω; Ly= 20 mH; Iy= 1 App)



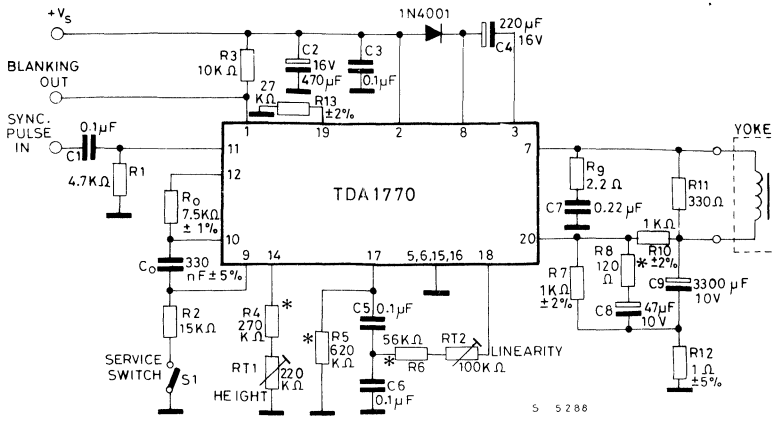
* The value depends on the characteristics of the CRT. The value shown is indicative only.

Typical performance

V_s	Minimum supply voltage	20	V
I_s	Supply current	160	mA
t_{fly}	Flyback time	0.75	msec
t_{blkg}	Blanking time	1.4	msec
f_o	Free running frequency	43.5	Hz
P_{tot}	Power dissipation	2.1	W
$R_{th\ heatsink}$ **	Thermal resistance of the heatsink for T_{amb}= 60°C and $T_{j\ max}$= 130°C	11	°C/W

** See "Thermal considerations".

Fig. 5 - Typical application circuit for small screen (Ry= 2.9Ω ; Ly= 6 mH; Iy= 1.1 App)



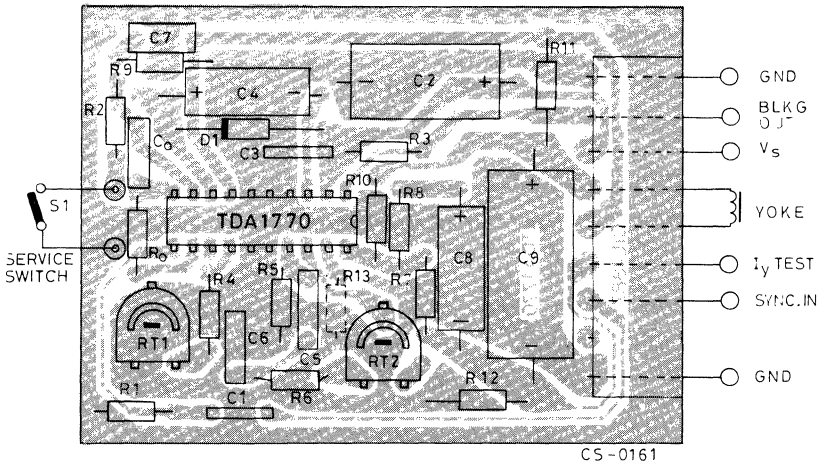
* The value depends on the characteristics of the CRT. The value shown is indicative only.

Typical performance

V_s	Minimum supply voltage	10.5	V
I_s	Supply current	170	mA
t_{fly}	Flyback time	0.45	msec
t_{blkg}	Blanking time	1.4	msec
f_o	Free running frequency	43.5	Hz
P_{tot}	Power dissipation	1.25	W
$R_{th\ heatsink}$ **	Thermal resistance of the heatsink for T_{amb}= 60°C and $T_{j\ max}$= 130°C	28	°C/W

** See "Thermal considerations".

Fig. 6 - PC board and components layout for the application circuits of fig. 3, 4 and 5 (1:1 scale)



APPLICATION INFORMATION (Refer to the block diagram)

Oscillator and Sync gate (Clock generation)

The oscillator is obtained by means of an integrator driven by a two threshold circuit that switches Ro high or low so allowing the charge or the discharge of Co under constant current conditions.
The Sync input pulse at the Sync gate lowers the level of the upper threshold and than it controls the period duration. A clock pulse is generated.

Pin 10 is the inverting input of the amplifier used as integrator.
Pin 12 is the output of the switch driven by the internal clock pulse generated by the threshold circuits.
Pin 9 is the output of the amplifier.
Pin 11 is the input for sync pulses (positive).

Ramp generator and buffer stage

A current mirror, the current intensity of which can be externally adjusted, charges one capacitor producing a linear voltage ramp.
The internal clock pulse stops the ramp increasing by a very fast discharge of the capacitor; a new voltage ramp is immediately allowed.
The required value of the capacitance is obtained by means of the series of two capacitors, Ca and Cb, which allow the linearity control by applying a feedback between the output of the buffer and the tapping from Ca and Cb.

Pin 14 The resistance between pin 7 and ground defines the current mirror current and than the height of the scanning.
Pin 17 is the output of the current mirror that charges the series of Ca and Cb. This pin is also the input of the buffer stage.
Pin 18 is the output of the buffer stage and it is internally coupled to the inverting input of the power amplifier through R1.

APPLICATION INFORMATION (continued)

Power amplifier

This amplifier is a voltage-to-current power converter, the transconductance of which is externally defined by means of a negative current feedback.
The output stage of the power amplifier is supplied by the main supply during the trace period, and by the flyback generator circuit during the most of the duration of the flyback time. The internal clock turns off the lower power output stage to start the flyback.
The power output stage is thermally protected by sensing the junction temperature and then by putting off the current sources of the power stage.

Pin 20 is the inverting input of the amplifier. An external network, Ra and Rb, defines the DC level across Cy so allowing a correct centering of the output voltage. The series network Rc and Cc, in conjunction with Ra and Rb, applies at the feedback input pin 20 a small part of the parabola, available across Cy, and the AC feedback voltage, taken across Rf. The external components Rc, Ra and Rd, produce the linearity correction on the output scanning current Iy and their values must be optimized for each type of CRT.

Pin 19 is the non-inverting input. At this pin the non-inverting input reference voltage supplied by the voltage regulator can be measured.
This pin is used on a quasi-bridge configuration or on portable TVS.

Pin 7 is the output of the power amplifier and it drives the yoke by a negative slope current ramp Iy. Re and the Boucherot cell are used to stabilize the power amplifier.

Pin 8 the supply voltage of the power output stage is forced at this pin. During the trace time the supply voltage is obtained from the main supply voltage V_s by a diode, while during the retrace time this pin is supplied from the flyback generator.

Flyback generator

This circuit supplies both the power amplifier output stage and the yoke during the most of the duration of the flyback time (retrace).
The internal clock opens the loop of the amplifier and lets pin 1 floating so allowing the rising of the flyback. Crossing the main supply voltage at pin 2, the flyback pulse front end drives the flyback generator in such a way allowing its output to reach and overcome the main supply voltage, starting from a low condition forced during the trace period.
An integrated diode stops the rising of this output increase and voltage jump is transferred by means of capacitor Cf at the supply voltage pin of the power stage (pin 8).
When the current across the yoke changes its direction, the output of the flyback generation falls down to the main supply voltage and it is stopped by means of the saturated output darlington at a high level. At this time the flyback generator starts to supply the power amplifier output stage by a diode inside the device. The flyback generator supplies the yoke too.
Later, the increasing flyback current reaches the peak value and then the flyback time is completed: the trace period restarts. The output of the power amplifier (pin 7) falls under the main supply voltage and the output of the flyback generator is driven for a low state so allowing the flyback capacitor Cf to restore the energy lost during the retrace.

Pin 3 is the output of the flyback generator that, when driven, jumps from low to high condition. An external capacitor Cf transfers the jump to pin 8 (see pin 8).

Blanking generator and CRT protection

This circuit is a pulse shaper and its output goes high during the blanking period or for CRT protection.

APPLICATION INFORMATION (continued)

The input is internally driven by the clock pulse that defines the width of the blanking time when a flyback pulse has been generated. If the flyback pulse is absent (short circuit or open circuit of the yoke), the blanking output remains high so allowing the CRT protection.

Pin 1 is an open collector output where the blanking pulse is available.

Voltage regulator

The main supply voltage V_s is lowered and regulated internally to allow the required reference voltages for all the above described blocks.

Pin 2 is the main supply voltage input V_s (positive).
Pin 5, 6, 15, 16 are the GND pins or the negative input of V_s.

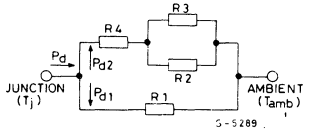
THERMAL CONSIDERATIONS (a note referred to Fig. 3, 4 and 5)

The shown value of case to ambient thermal resistance is the equivalent to three thermal resistances that are:

R1 – Thermal resistance junction to ambient of the device.
R2 – Thermal resistance of the p.c. copper side.
R3 – Thermal resistance of the auxiliary heatsink.

The circuit that contains these thermal resistances is shown on fig. 7 where R3 is the thermal resistance junction to pins of the device and Pd is the maximum dissipated power.

Fig. 7 - Semiconductor heatsink thermal circuit.



Since the thermal resistance R3 of the heatsink is defined from its physical and mechanical characteristics, it is necessary to define the required copper side on the p.c. board for the necessary R2 value. For instance, let's consider the application for the 90° yoke.
It is known:

$T_{j\ max}$= 130°C; $T_{amb\ max}$= 60°C; $R_{th\ c\text{-}amb}$= 8°C/W; $R_{th\ j\text{-}pins}$ (or R4)= 14°C/W; $R_{th\ j\text{-}amb}$= 80°C/W.

It can be calculated:

$$P_d = \frac{T_{j\ max} - T_{amb\ max}}{R_{th\ c\text{-}amb} + R_{th\ j\text{-}pins}} = \frac{130 - 60}{8 + 14} = 3.18W$$

Using an auxiliary heatsink of a thermal resistance R3= 20°C/W (including some losses), it can be easily calculated (see fig. 7): R2 = 94°C/W.
From fig. 9, it can be found: $\ell \geqslant 21$ mm.

MOUNTING INSTRUCTIONS

The $R_{th\ j\text{-}amb}$ of the TDA 1770 can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Fig. 8) or to an external heatsink.
The diagram of figure 9 shows the R_{th} as a function of the side "ℓ" of two equal square copper areas having a thickness of 35μ (1.4 mils).
During soldering the pins temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.
The external heatsink or printed circuit copper area must be connected to electrical ground.

Fig. 8 - Example of P.C. board copper area which is used as heatsink.

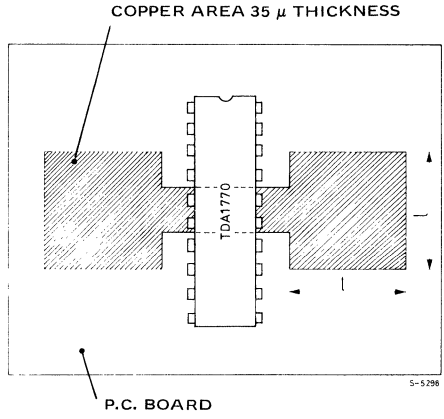


Fig. 9 - Thermal resistance of the P.C. copper side vs. side "ℓ"

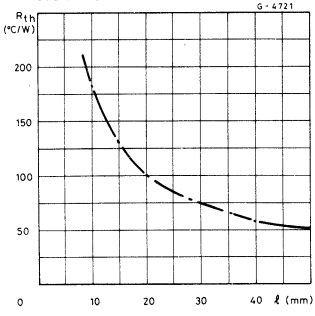


Fig. 10 - Maximum allowable power dissipation vs. ambient temperature